

WHAT CLAIMED IS:

1 1. An integrated circuit system having a plurality of macros, said integrated
2 circuit comprising:
3 an external voltage supply input configured for supplying an external voltage to
4 the integrated circuit; and
5 a plurality of internal voltage supply generators, each of the plurality of internal
6 voltage supply generators being connected to a respective macro of the plurality of
7 macros and configured for receiving the external voltage via the external voltage supply
8 input for generating an internal voltage supply for operating its respective macro, wherein
9 each of the plurality of internal voltage supply generators includes circuitry for
10 generating the internal voltage supply and circuitry for disconnecting at least a portion of
11 its respective macro.

1 2. The integrated circuit system as in claim 1, wherein each of the plurality
2 of internal voltage supply generators regulate the internal voltage supply generated there
3 from.

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1 3. The integrated circuit system as in claim 1, wherein the external voltage
2 is greater than the internal voltage supply.

1 4. The integrated circuit system as in claim 1, further comprising a scan-
2 chain formed by a chain of scannable register latches storing fuse information and a
3 switch enable/disable signal.

1 5. The integrated circuit system as in claim 1, wherein each of the plurality
2 of internal voltage supply generators comprise a reference voltage generator for
3 generating and providing a reference voltage for driving at least one voltage generator.

1 6. The integrated circuit system as in claim 6, wherein the reference voltage
2 generator and the at least one voltage generator provide voltage to a substrate bias level
3 voltage generator, a negative word line level voltage generator, and a boosted wordline
4 high level voltage generator.

1 7. The integrated circuit system as in claim 1, wherein the circuitry for
2 generating the internal voltage supply comprises:
3 a reference supply unit for generating at least one of a voltage level and current
4 level;
5 a voltage limiter coupled to the reference supply unit for controlling a voltage
6 output level outputted from the voltage limiter;
7 an oscillator coupled to the voltage limiter for receiving the voltage output level
8 and generating an oscillating voltage level; and
9 a charge pump for receiving the oscillating voltage level for generating the
10 internal voltage supply.

1 8. The integrated circuit system as in claim 7, wherein a feedback voltage
2 is provided from the charge pump to the voltage limiter.

1 9. The integrated circuit system as in claim 7, wherein the external voltage
2 drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

1 10. The integrated circuit system as in claim 7, wherein the circuitry for
2 generating the internal voltage supply further comprises an enable register coupled to the
3 voltage limiter, the oscillator and the charge pump, wherein the enable register is
4 configured for storing one of an enable and disable signal and for enabling or disabling at
5 least the voltage limiter, the oscillator and the charge pump according to the stored signal.

1 11. The integrated circuit system as in claim 10, wherein the enable register
2 stores one of the enable and disable signal during a power-on period.

1 12. An integrated circuit system having a plurality of macros, said integrated
2 circuit comprising:
3 means for receiving an external voltage;
4 means coupled to the means for receiving the external voltage for generating an
5 internal voltage supply for operating at least one of a plurality of internal voltage supply
6 generators coupled to a respective macro of the plurality of macros; and
7 means for controlling the means coupled to the means for receiving the external
8 voltage according to an enable/disable signal to selectively connect and disconnect at
9 least a portion of the respective macro of the plurality of macros.

1 13. The integrated circuit system as in claim 12, further comprising a scan-
2 chain formed by a chain of scannable register latches storing fuse information and the
3 enable/disable signal.

1 14. The integrated circuit system as in claim 12, wherein the means coupled
2 to the means for receiving the external voltage comprise a reference voltage generator for
3 generating and providing a reference voltage for driving at least one voltage generator.

1 15. The integrated circuit system as in claim 14, wherein the reference
2 voltage generator and the at least one voltage generator provide voltage to the at least one
3 of the plurality of internal voltage supply generators.

1 16. The integrated circuit system as in claim 12, wherein the at least one of
2 the plurality of internal voltage supply generators is selected from the group consisting of
3 a substrate bias level voltage generator, a negative word line level voltage generator, and
4 a boosted wordline high level voltage generator.

1 17. The integrated circuit as in claim 12, wherein the means coupled to the
2 means for receiving the external voltage comprises:

3 a reference supply unit for generating at least one of a voltage level and current
4 level;

5 a voltage limiter coupled to the reference supply unit for controlling a voltage
6 output level outputted from the voltage limiter;

7 an oscillator coupled to the voltage limiter for receiving the voltage output level
8 and generating an oscillating voltage level; and

9 a charge pump for receiving the oscillating voltage level for generating the
10 internal voltage supply.

1 18. The integrated circuit system as in claim 17, wherein a feedback voltage
2 is provided from the charge pump to the voltage limiter.

1 19. The integrated circuit system as in claim 17, wherein the external voltage
2 drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

1 20. The integrated circuit system as in claim 17, wherein the means for
2 controlling the means coupled to the means for receiving the external voltage according
3 to the enable/disable signal comprises at least one enable register coupled to the voltage
4 limiter, the oscillator and the charge pump, wherein the at least one enable register is
5 configured for storing the enable/disable signal and for enabling or disabling at least the
6 voltage limiter, the oscillator and the charge pump according to the stored enable/disable
7 signal.

1 21. The integrated circuit system as in claim 12, wherein at least one enable
2 register stores the enable/disable signal during a power-on period.

1 22. The integrated circuit system as in claim 20, further comprising means
2 for performing a built-in self test for testing the DC voltage generator system.